PAD STRUCTURE OF SEMICONDUCTOR DEVICE FOR REDUCING OR INHIBITING WIRE BONDING CRACKS

BACKGROUND OF THE INVENTION

Field of the Invention

[0001] The invention relates in general to a pad structure of semiconductor device, and more particularly to an improved pad structure of semiconductor device for reducing wire bonding cracks.

Description of the Related Art

[0002] Light, small and easy to carry electronic product is a leading trend of modern living. Chip-On-Board (COB) technology has become one of common technique in the fabrication of modern electronic product, and wire bonding and molding procedures are the key steps in COB technique. Generally, COB technology consists of three semiconductor die to printed circuit board conductive attachment techniques: wire bonding, flip chip attachment and tape automated bonding (TAB).

[0003] The bond wires are generally attached through one of three industry-standard wire bonding techniques: ultrasonic bonding--using a combination of pressure and ultrasonic vibration bursts to form a metallurgical

cold weld; thermocompression bonding--using a combination of pressure and elevated temperature to form a weld; and thermosonic bonding--using a combination of pressure, elevated temperature, and ultrasonic vibration bursts.

[0004] Thus, as the semiconductor device is subjected to the normal stresses of subsequent forming and assembly operations (such as bonding pressure), parts of device structure may crack, especially the interface between VIA window and Inter-metal dielectric layer (IMD).

[0005] Fig. 1A is a cross-sectional view of a portion of a conventional semiconductor device. In order to clarify the technical differences between the prior art and the invention, the drawings in the context of the invention only show the major characteristic parts of the semiconductor device. Beneath the metallic layers, the semiconductor device 100 comprises a silicon substrate 102, a field oxide layer 104 and an inter-layer dielectrics 106, as shown in Fig. 1A. The silicon substrate 100 has a p-well region or/ and an n-well region beneath (not shown); for example, a p-well is formed by diffusion or ion implantation of boron into the silicon substrate 102, as well known in the art. A complete integrated circuit (IC) device consists of numerous MOS transistor. Several dielectric layers should be formed in the IC device for the purpose of isolation; for example, the field oxide (commonly termed "FOX")

layer 104 is used for the isolation of the adjacent transistors, and the inter-layer dielectric (commonly termed "ILD") layer 106 is used for the isolation between the metallic layer and the substrate 102. Borophosphosilicate glass (BPSG) is typically used as the material of the ILD layer 106, and can be formed over the substrate 102 and the FOX layer 104 by thermal chemical vapor deposition (CVD) process, as known in the art. Subsequently, the metallic layer deposition is performed.

[0006] Single or multi metallic layers can be deposited above the ILD layer 106, depending on the requirement of semiconductor device. In Fig. 1A, three metallic layers, including the first metallic layer 108, the second metallic layer 114 and the third metallic layer 120, are taken for illustration. Also, an inter-metal dielectric (commonly termed "IMD") layer and several via holes are formed between two metallic layers. Those via holes are typically filled with metal such as tungsten (W).

[0007] According to the illustration of Fig. 1, there are a first IMD layer 110 and several first via holes 112 formed between the first metallic layer 108 and the second metallic layer 114. A second IMD layer 116 and several second via holes 118 are formed between the second metallic layer 114 and the third metallic layer 120. All of the first via holes 112 and second via holes 118 are filled with tungsten (W), to contact the associated metallic layers both

mechanically and electrically. Silicon oxides (SiO_2) is a typical material of the first IMD layer 110 and the second IMD layer 116, and can be formed by plasma-enhanced chemical vapor deposition (PECVD), or high-density-plasma chemical vapor deposition (HDP-CVD) process.

[0008] Fig. 1B is a top view of the IMD layer and via holes of Fig. 1A. Fig. 1C is a diagrammatic oblique view of the second via holes of Fig. 1A after wire bonding. The arrangement of the second via holes 118 in the second IMD layer 116 is like the pins sticking into the pincushion, as shown in Fig. 1B and Fig. 1C. Because the material (such as silicon oxide) of the second IMD layer 116 is much more fragile than metal such as tungsten filled in the via holes 118, the interface between the IMD and metal is easily broken under the wire-bonding pressure. Those cracks 171, 172, and 173 as shown in Fig. 1C are so-called "pad cracks".

[0009] Also, since the conventional via holes are arranged like the pins in the pincushion, the IMD layer interposed between two metallic layers can be treated as a continuous substance. The crack generated under the bonding pressure is free to extend until it hits the interface between the IMD and via contact (via hole filled with tungsten). Thus, the unstoppable cracks, such as the longer cracks 171 and 173 of Fig. 1C, are the typical problem when wire bonding the semiconductor device with the conventional pad structure. If an

IC chip having the pad crack defect is installed in the electronic product, some problems, for example, current leakage, occur as expected.

SUMMARY OF THE INVENTION

[0010] It is therefore an object of the invention to provide a pad structure of semiconductor device with a special via pattern, so as to reduce or completely inhibit the wire bonding cracks.

[0011] The invention achieves the first objects by providing a pad structure of semiconductor device for reducing wire bonding crack. The device comprises a substrate; an inter-layer dielectric (ILD) layer formed over the substrate; a plurality of metallic layers formed over the ILD layer; and a plurality of inter-metal dielectric (IMD) layers. Each IMD layer is formed between two metallic layers, and has a plurality of via holes. At least one of IMD layers is divided into a plurality of separated IMD blocks by the via holes formed therein, which the via holes contact one metallic layer closest to a pad bonding layer.

[0012] The invention achieves the second first objects by providing a pad structure of semiconductor device for completely inhibiting wire bonding crack. The device comprises a substrate; an inter-layer dielectric (ILD) layer formed over the substrate; a plurality of metallic layers formed over the ILD layer; and

a plurality of inter-metal dielectric (IMD) layers. Each IMD layer is formed between two metallic layers, and has a plurality of via holes. At least two of IMD layers are divided into a plurality of separated IMD blocks by the via holes formed therein. Also, one of at least two IMD layer is preferably close to a pad bonding layer.

[0013] Other objects, features, and advantages of the invention will become apparent from the following detailed description of the preferred but non-limiting embodiments. The following description is made with reference to the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

[0014] Fig. 1A (prior art) is a cross-sectional view of a portion of a conventional semiconductor device;

[0015] Fig. 1B (prior art) is a top view of the IMD layer and via holes of Fig. 1A;

[0016] Fig. 1C (prior art) is a diagrammatic oblique view of the second via holes of Fig. 1A after wire bonding;

[0017] Fig. 2 is a diagrammatic oblique view of a portion of a semiconductor device in accordance with the first embodiment of the

invention;

[0018] Fig. 3 is a diagrammatic oblique view of a portion of a semiconductor device in accordance with the second embodiment of the invention; and

[0019] Fig. 4A~Fig. 4L are the top views of the via holes of Pat. 1~Pat. 12 in Experiments 2 and 3, respectively.

DETAILED DESCRIPTION OF THE INVENTION

[0020] In the present invention, the inter-metal dielectric (IMD) layer is divided into several individual IMB blocks by a special via pattern, in order to reduce or completely inhibit the wire-bonding crack phenomenon. The details of the invention are described by two embodiments. In the first embodiment, a single IMD layer with a special via (hole) pattern is constructed to reduce the wire-bonding cracks. In the second embodiment, two IMD layers with a special via (hole) pattern in each are constructed to inhibit the wire-bonding cracks.

[0021] Also, the drawings used for illustrating the embodiment of the invention only show the major characteristic parts of the semiconductor device in order to avoid obscuring the invention. Accordingly, the specification and

the drawing are to be regard as an illustrative sense rather than a restrictive sense.

First Embodiment

[0022] Fig. 2 is a diagrammatic oblique view of a portion of a semiconductor device in accordance with the first embodiment of the invention. Beneath the metallic layers, the semiconductor device 200 comprises a silicon substrate 202, a field oxide layer 204 and an inter-layer dielectrics 206. The silicon substrate 200 has a p-well region or/ and an n-well region beneath (not shown); for example, a p-well is formed by diffusion or ion implantation of boron into the silicon substrate 202, as well known in the art. The field oxide (commonly termed "FOX") layer 204 is used for the isolation of the adjacent transistors (not shown), and the inter-layer dielectric (commonly termed "ILD") layer 206 is used for the isolation between the metallic layer and the substrate 202. Borophosphosilicate glass (BPSG) is a typical material of the ILD layer 206, and can be formed over the substrate 202 and the FOX layer 204 by thermal chemical vapor deposition (CVD) process. Subsequently, the metallic layer deposition is performed.

[0023] Single or multi metallic layers can be deposited above the ILD layer 206, depending on the requirement of semiconductor device. In the first

embodiment, three metallic layers, including the first metallic layer 208, the second metallic layer 214 and the third metallic layer 220, are used for illustration. Also, an inter-metal dielectric (commonly termed "IMD") layer and several via holes are further formed between two metallic layers. Those via holes are typically filled with metal such as tungsten (W).

[0024] In Fig. 2, a first IMD layer 210 and several first via holes 212 are formed between the first metallic layer 208 and the second metallic layer 214. A second IMD layer 216 and several second via holes 218 are formed between the second metallic layer 214 and the third metallic layer 220. All of the first via holes 212 and second via holes 218 are filled with tungsten (W), in order to contact the associated metallic layers both mechanically and electrically. Silicon oxides (SiO_2) is a typical material of the first IMD layer 210 and the second IMD layer 216, and can be formed by plasma-enhanced chemical vapor deposition (PECVD), or high-density-plasma chemical vapor deposition (HDP-CVD) process.

[0025] In the first embodiment, only one IMD layer having a special via pattern is constructed to reduce the wire bonding cracks. This "special" IMD layer is preferably at the position close to the bonding pads, for effectively buffering the impact of a bonding force (the closer, the better). In Fig. 2, the second IMD layer 216 is the "special" IMD layer of the invention, and the

second via holes 218 compose a special via pattern.

[0026] As shown in Fig. 2, the top surfaces of the second via holes 218 compose a chessboard pattern, and the second IMD layer 216 is divided into a plurality of separated IMD blocks by the second via holes 218. It has been proved (see Experiment 2) that those separated IMD blocks can effectively stop the cracks from wild extension after impacted by the bonding force, even the cracks occur at the interface between the second via hole (filled with W) 218 and the IMD layer (SiO_2) 216.

[0027] It is noted that the special via pattern is not limited to the chessboard pattern as shown in Fig. 2, it could be any patterns which can turn the IMD layer into several individual IMD blocks, such as a pattern in a form of concentric frames, concentric circles, or spider web.

Second Embodiment

[0028] In the second embodiment, two IMD layers with a special via (hole) pattern in each are constructed. It has been proved (see Experiment 3) that those separated IMD blocks of two IMD layers can completely inhibit the wire bonding cracks.

[0029] Fig. 3 is a diagrammatic oblique view of a portion of a

semiconductor device in accordance with the second embodiment of the invention. Components common to Fig. 2 retain the same numeric designation. Beneath the metallic layers, the semiconductor device 300 comprises a silicon substrate 202, a field oxide (commonly termed "FOX") layer 204 and an inter-layer dielectrics 206. Borophosphosilicate glass (BPSG) is a typical material of the ILD layer 206, and can be formed over the substrate 202 and the FOX layer 204 by thermal chemical vapor deposition (CVD) process. Single or multi metallic layers can be deposited above the ILD layer 206, depending on the requirement of semiconductor device. In the second embodiment, three metallic layers, including the first metallic layer 208, the second metallic layer 214 and the third metallic layer 220, are used for illustration.

[0030] Also, a first IMD layer 210 and several first via holes 312 are formed between the first metallic layer 208 and the second metallic layer 214. A second IMD layer 216 and several second via holes 318 are formed between the second metallic layer 214 and the third metallic layer 220. All of the first via holes 312 and second via holes 318 are filled with tungsten (W), in order to contact the associated metallic layers both mechanically and electrically. Silicon oxides (SiO_2) is a typical material of the first IMD layer 210 and the second IMD layer 216, and can be formed by plasma-enhanced chemical

vapor deposition (PECVD), or high-density-plasma chemical vapor deposition (HDP-CVD) process.

[0031] In the second embodiment, two IMD layers both having the special via pattern is constructed to inhibit the wire bonding cracks. Those individual IMD blocks of the first and second IMD layers do increase the stress area, and consequently decrease the wire-bonding stress applied to IMD layer. Also, the results of the wire bonding experiment (Experiment 3) indicate that the device structure according to the second embodiment of the invention is capable of inhibiting the wire bonding cracks.

[0032] It is noted that the special via pattern is not limited to the concentric frames as shown in Fig. 3, it could be any patterns which can divide the IMD layer into several individual IMD blocks, such as a pattern in a form of chessboard, concentric circles, or spider web.

[0033] It is, of course, understood that a number of configuration of this embodiment could be constructed, including stacks of more than two IMD layers having individual IMD blocks, or stacks of more than three metallic layers. Those "special" IMD layers are preferably at the positions close to the bonding pads, for completely buffering the impact of a bonding force (the closer, the better).

[0034] Moreover, the first via pattern (formed by the top surfaces of the first via holes 312) could be, or could be not identical with the second via pattern (formed by the top surfaces of the first via holes 318). Also, the individual IMD blocks of the first and second IMD layer could be aligned, or staggered with each other.

Wire Bonding Experiment

Experiment 1 : Two IMD layers having pin-like via holes (Comparative Exp.)

[0035] A wire bonding experiment of conventional pad structure having VIA 1 STD/ VIA 2 STD (i.e. the first via holes arranged in the standard pin-like form/ the second via holes arranged in the standard pin-like form) is conducted for comparison. Please also refer to Fig. 1A~Fig. 1C for the demonstration of pad structure of Experiment 1. In Experiment 1, it is investigated if altering the wire boding parameters has an effect on the reduction of the wire bonding cracks. The results are summarized in Table 1.

[0036] The results of Table 1 indicated that more cracks occurred while increase the bonding power. Although less cracks were observed while decreasing the bonding power, the device fails in wire pull test. Accordingly, altering the wire boding parameters has no substantial effect on the reduction of the wire bonding cracks.

Experiment 2 : One IMD layer having a via pattern of the invention

[0037] A wire bonding experiment of a pad structure having VIA 1 STD/ VIA 2 experimental pattern (i.e. the first via holes arranged in the standard pin-like form/ the second via holes arranged in a special pattern of the invention) is conducted. Please also refer to Fig. 2 for the demonstration of pad structure of Experiment 2. In Experiment 2, it is investigated if a single IMD layer with several individual IMD blocks has an effect on the reduction of the wire bonding cracks. The results are summarized in Table 2. The top view of the via patterns are depicted in Fig. 4A~Fig. 4L, respectively. In Fig. 4A~Fig. 4L, the dark area represents the top view of the via holes filled with tungsten, and the empty area with no marking represents the top view of the IMD layer. Also, the top view of the via holes of sample no. Pat. 2~Pat. 6 (Fig. 4B~Fig. 4F) are all in a form of chessboard, except the widths of the via and IMD block are different.

[0038] The results of Table 2 indicated that the pad structure with a single via pattern does effectively reduce the wire bonding cracks.

Exp rim nt 3 : Two IMD layers both having a via pattern of the invention

[0039] A wire bonding experiment of a pad structure having VIA 1 experimental pattern / VIA 2 experimental pattern (i.e. the first via holes and the second via holes all arranged in a special pattern of the invention) is conducted. In this experiment, the VIA 1 pattern is identical with the VIA 2 pattern. Please also refer to Fig. 3 for the demonstration of pad structure of Experiment 3. It is investigated if two IMD layers with several individual IMD blocks have an effect on the completely inhibition of the wire bonding cracks herein. The results are summarized in Table 3. Also, the top view of the via patterns are depicted in Fig. 4A~Fig. 4L, respectively. In Fig. 4A~Fig. 4L, the dark area represents the top view of the via holes filled with tungsten, and the empty area with no marking represents the top view of the IMD layer. The top view of the via holes of Pat. 2~Pat. 6 (Fig. 4B~Fig. 4F) are all in the chessboard-like form, except the widths of the via and IMD block are different.

[0040] The vias having the top surfaces of Pat. 2, Pat. 3, Pat. 5, Pat. 6, Pat. 9 and Pat. 11 can divide the IMD layer into several individual IMD blocks, and successfully pass the bonding examine without peeling and cracking. Accordingly, the results of Table 3 indicated that the pad structure with two layers of special via patterns of the invention does completely inhibit the wire bonding cracks.

[0041] In the aforementioned description, the via with a special pattern which divides the IMD layer into several individual IMD blocks could restrict the crack path from wild spread, and consequently decrease the possibility of crack generation. According to the experimental results, the pad structure with a single via pattern of the invention does effectively reduce the wire bonding cracks, and the pad structure with two layers of special via patterns of the invention does completely inhibit the wire bonding cracks. Consequently, the yield of semiconductor device is greatly increased.

[0042] While the invention has been described by way of examples and in terms of the preferred embodiments, it is to be understood that the invention is not limited thereto. On the contrary, it is intended to cover various modifications and similar arrangements and procedures, and the scope of the appended claims therefore should be accorded the broadest interpretation so as to encompass all such modifications and similar arrangements and procedures.